Effect of Underfill on CSP Assembly Reliability

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California
818-354-2059, Reza.Ghaffarian@jpl.nasa.gov

ABSTRACT

This presentation reviews the package trend towards miniaturization via chip scale packages (CSPs). The industry definition of CSP has steadily evolved as technology and infrastructure for finer pitch has become more readily available. To keep up with the definition, CSPs are considered to be miniature new packages that industry is starting to implement, and there are many unresolved technical issues associated with their implementation. One key issue yet to be fully addressed is the CSP interconnect reliability and the effects of manufacturing variables. Understanding quality and assembly reliability issues associated with the implementation of CSPs were the main objectives of the JPL-led CSP Consortium with representatives from government agencies and private companies. The Consortium experience gained in the process of building 150 test vehicles with eleven CSPs in the areas of technology implementation challenges is presented. This includes the design and building of both standard and microvia boards, and the assembly of two types of test vehicles. Several assemblies were underfilled to determine the impact of underfill on the level of reliability improvements. Thermal cycle test results under four environmental conditions for assemblies with and without underfills are also presented.